IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A signal processor comprising:

a plurality of function blocks configured to perform signal processing, each function block comprising one or more devices which collectively perform a specified function of the signal processor;

a plurality of dedicated paths configured to transmit debug information for debugging the signal processor, the debug information obtained from respective function blocks of the plurality of function blocks;

a selection multiplex output block connected to the plurality of dedicated paths and configured to input the debug information via the dedicated paths, and output the inputted debug information;

a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block; and

at least two of the dedicated paths are provided ~~for one of the plurality of~~ to connect the at least one of the function blocks with the selection multiplex output block such that the selection multiplex output block has at least two inputs from the at least one of the function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with ~~said one of the plurality of~~ the at least one of the function blocks, as the debug information, from ~~said one of the plurality of~~ the at least one of the function blocks to the selection multiplex output block in response to the instruction from the processing unit.

Claim 2 (Previously Presented): The signal processor according to claim 1, wherein the dedicated paths transmit the debug information serially.

Claim 3 (Previously Presented): The signal processor according to claim 1, wherein the debug information includes the input data associated with said one of the plurality of function blocks.

Claim 4 (Previously Presented): The signal processor according to claim 1, wherein the debug information includes the output data associated with said one of the plurality of function blocks.

Claim 5 (Previously Presented): The signal processor according to claim 1, wherein the debug information is data in an arbitrary size.

Claim 6 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system,

wherein one of the plurality of function blocks is an error correction coder block, which inputs transmission data for coding as input data, performs error correction coding as the signal processing, and outputs a coded data series as output data.

Claim 7 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is a modulator block, which inputs a coded data series as input data, performs modulation as the signal processing, and outputs modulated transmission data as output data.

Claim 8 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is a demodulator block, which inputs received modulated data as input data, performs demodulation as the signal processing, and outputs a demodulated data series as output data.

Claim 9 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is an error correction decoder block, which inputs a decoded data series as input data, performs error bit correction as the signal processing, and outputs decoded data as output data.

Claim 10 (Previously Presented): The signal processor according to claim 1, wherein the selection multiplex output block is further configured to acquire an instruction from an outside of the signal processor, select the debug information based on the instruction acquired, input the debug information selected via a dedicated output path, and output the inputted debug information to the outside of the signal processor.

Claim 11 (Previously Presented): The signal processor according to claim 10, wherein the selection multiplex output block selects multiple pieces of debug information based on the instruction, inputs the multiple pieces of debug information, multiplexes the multiple pieces of debug information, and outputs multiplexed debug information to the outside of the signal processor.

Claim 12 (Original): The signal processor according to claim 11, wherein the multiple pieces of debug information are acquired from different function blocks.

Claim 13 (Original): The signal processor according to claim 10, wherein the selection multiplex output block performs time multiplexing.

Claim 14 (Original): The signal processor according to claim 1, wherein the debug information is added with time information.

Claim 15 (Original): The signal processor according to claim 14, wherein the time information is added by a function block.

Claim 16 (Original): The signal processor according to claim 15, wherein the time information includes a plurality of frame counters of different cycles.

Claim 17 (Original): The signal processor according to claim 16, wherein the plurality of frame counters includes CFN (Connection Frame Number Counter) and BFN (Node B Frame Number Counter).

Claim 18 (Previously Presented): The signal processor according to claim 1, wherein the at least two dedicated paths comprise a first path configured to transmit the input data and a second path configured to transmit the output data.

Claim 19 (Previously Presented): The signal processor according to claim 1, further comprising:

a memory disposed inside the one of the plurality of function blocks.

Claim 20 (Previously Presented): The signal processor according to claim 1, further comprising:

at least one of a digital signal processor (DSP), a large scale integration (LSI) chip, and a field programmable gate array (FPGA) included in the plurality of function blocks.